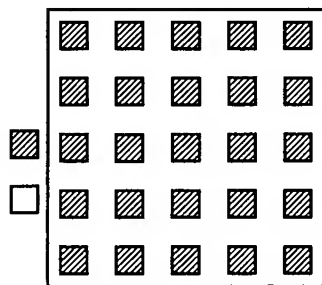


Title: High Density Integrated Circuits And The Method Of Packaging The Same

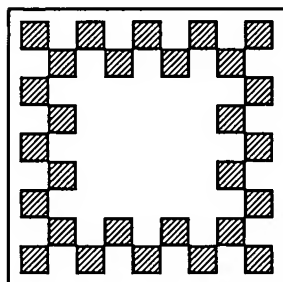
Applicant: Daniel Wang

Application No.: 10/057,448

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Prior Art
Figure 1
Perimeter I/O



Prior Art
Figure 2
Staggered Perimeter I/O

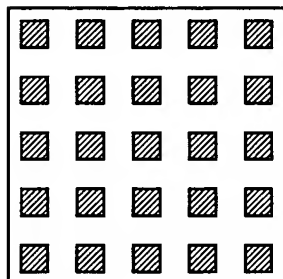


Figure 3
Full Array

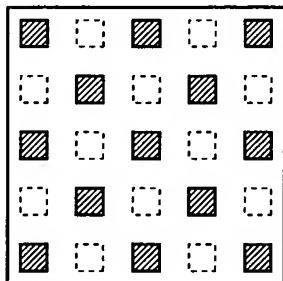


Figure 4
Depopulated Array

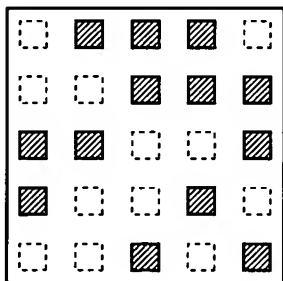


Figure 5
Random Array

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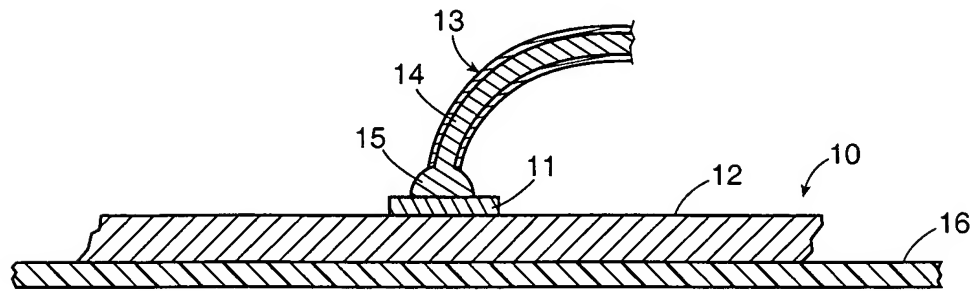


Figure 6

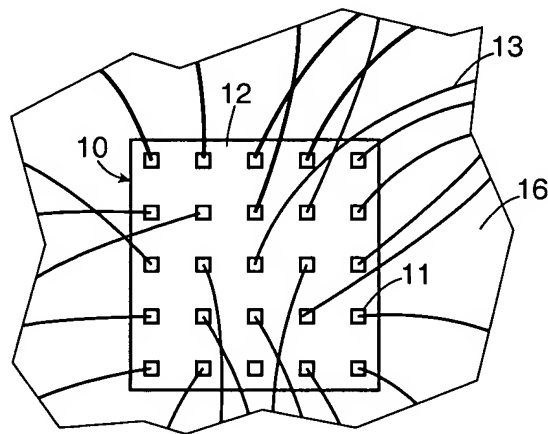


Figure 7

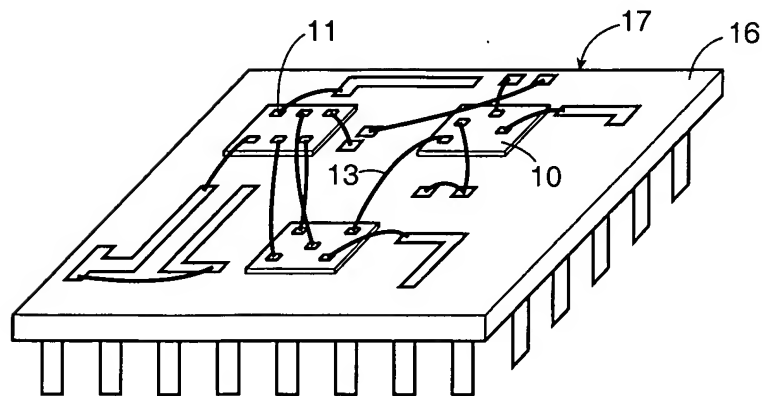


Figure 8

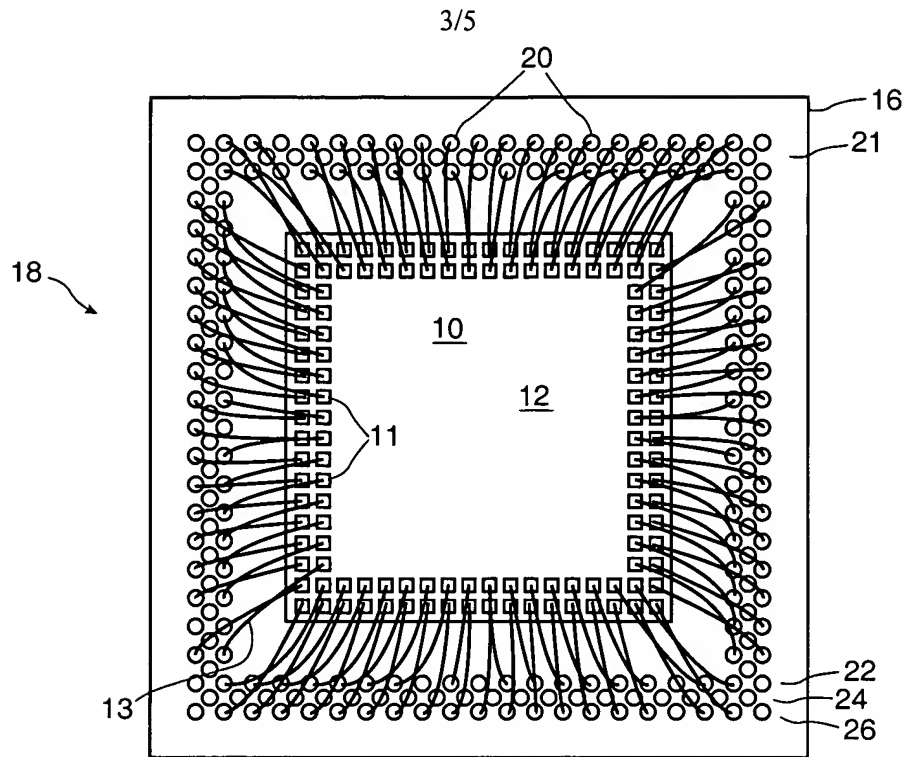


Figure 9

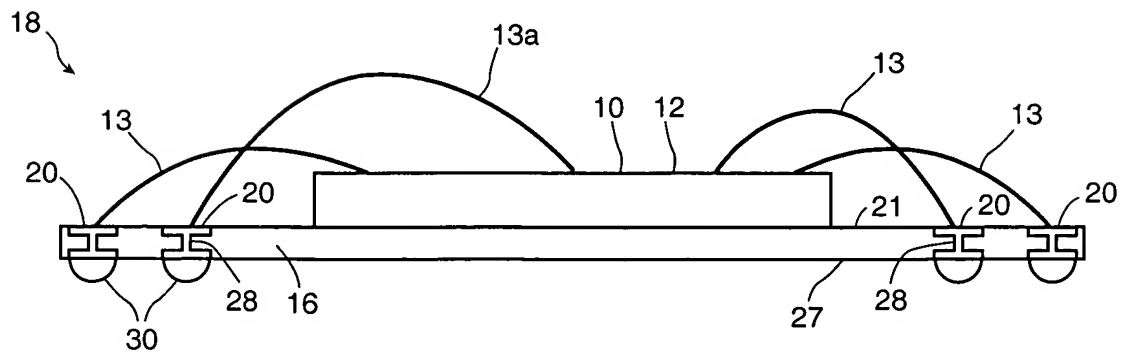


Figure 10

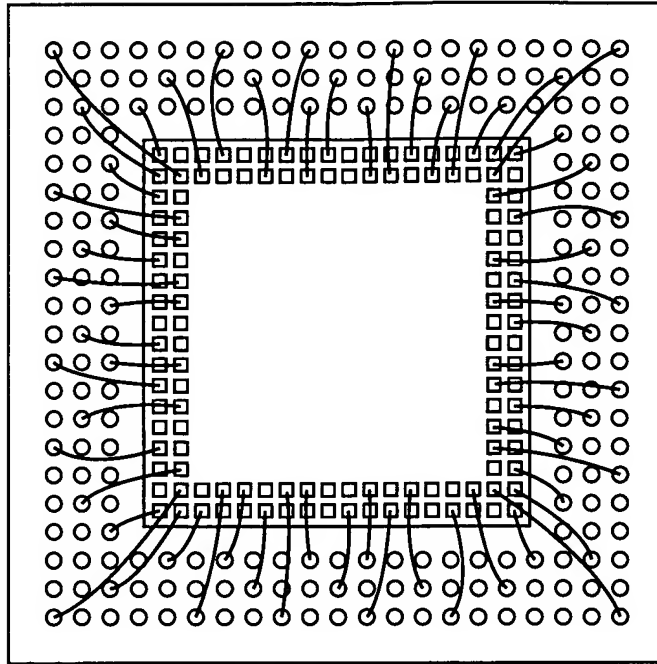


Figure 11b

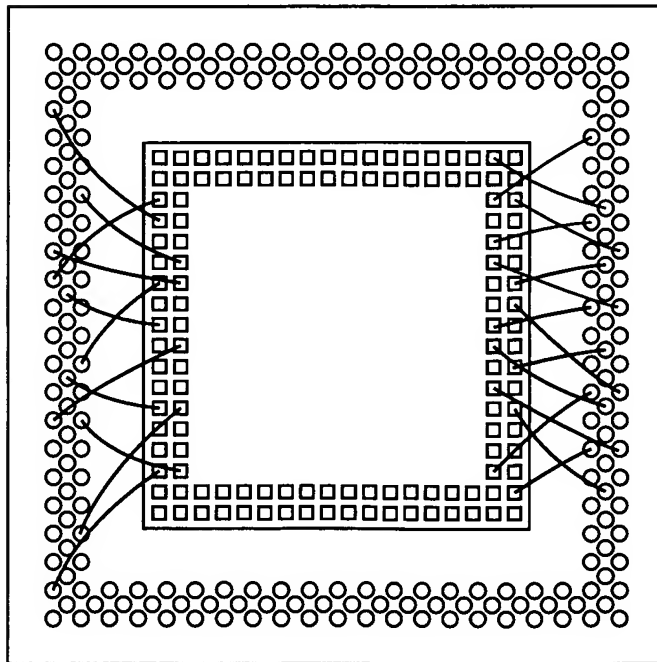


Figure 11a

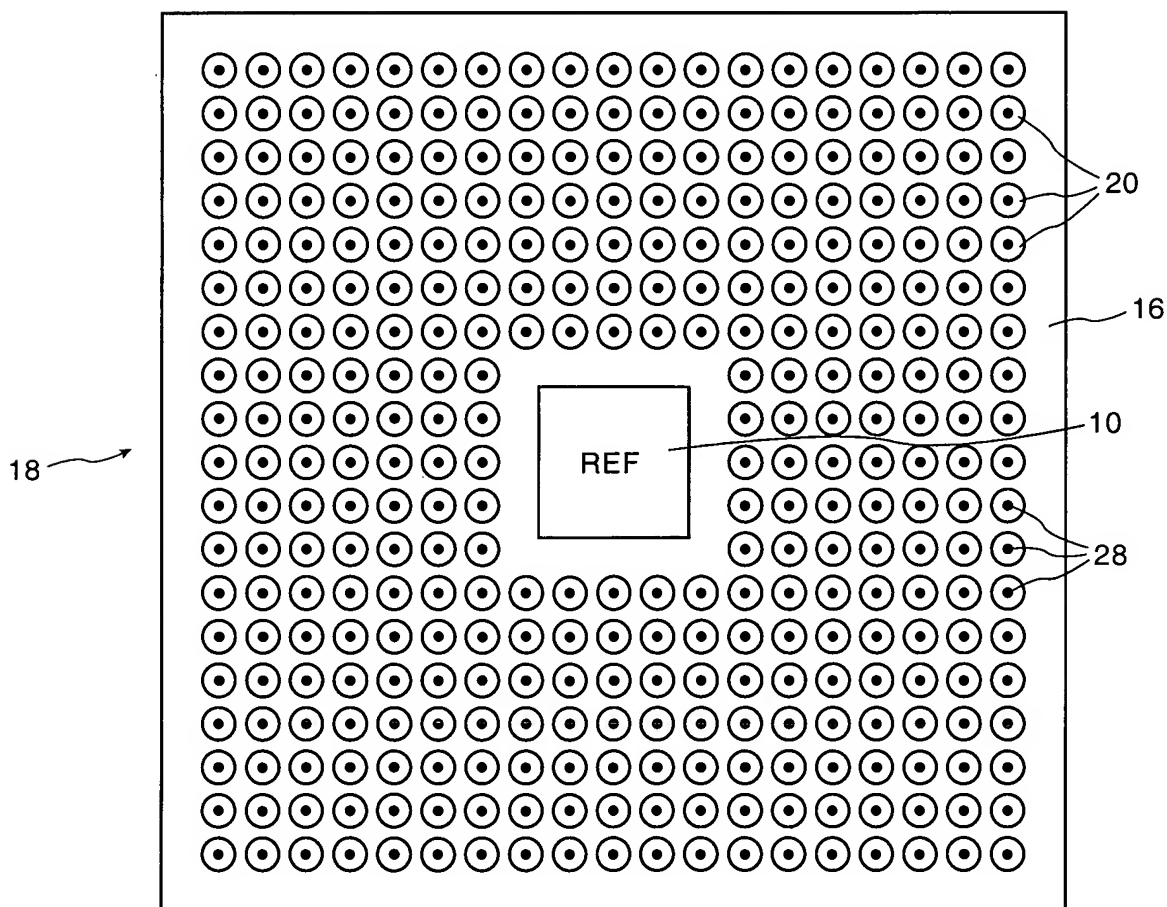


Figure 12